LOW PROFILE STACKED MULTI-CHIP PACKAGE AND METHOD OF FORMING SAME

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a divisional of, and claims priority from, U.S. Patent Application Serial No. 09/968,365, filed September 30, 2001, and ~~currently pending.~~ now US Patent 6,696,320

TECHNICAL FIELD

This disclosure relates generally to integrated circuits, and in particular but not exclusively, relates to integrated circuit packaging.

BACKGROUND

Many integrated circuits (*i.e.*, chips) have a need for a large number of input and/or output (I/O) connections off the chip. However, typical chips use the periphery of the chip to provide I/O connections, which works well with conventional wire bonding technology to implement the off-chip connections. Relatively new flip chip technology can be used to provide an increased number of I/O connections on the circuit side of the chip. Flip chips typically use conductive "bumps" formed on the surface of the circuit side of the flip chip, which are used to make off-chip connections to corresponding conductive regions on an interconnect substrate (*e.g.*, ceramic, flexible tape), or printed wiring board or other interconnect structure.

However, the demand continues for even more I/O connections. At the same time, users typically desire a thin profile or pitch when the chips are